## REMARKS

Claims 1-4 are pending in the application.

Claims 1-4 are rejected.

Claims 1-4 are rejected under 35 U.S.C. 112.

Claims 1-4 are rejected under 35 U.S.C. 103(a).

Claims 5-8 have been added.

No new matter is added.

Claims 1-8 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

### *Claim Rejections – 35 U.S.C. § 112*

Claims 1-4 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The applicant has amended claims 1 and 3 as per the Examiner's recommendations. In particular, claim 1 has been amended to specify "providing a substrate having a chip mounted thereon, the substrate having an upper surface..." as suggested by the examiner. Claim 1 has also been amended to replace "forming a solder preform" with "arranging a solder preform" to clarify the formation/preformed issue raised by the Examiner. Claim 3 has also been amended to replace "The semiconductor package of any of claim 1" with "The method of claim 1" as suggested by the Examiner.

### *Claim Rejections – 35 U.S.C. § 103*

Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,437,240 to Smith (hereafter "Smith '240") in view of U.S. Patent No. 5,747,102 to Smith, et al. (hereafter "Smith '102").

Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Smith '240 in view of Smith '102 as applied to claim 1 above, and further in view of U.S. Patent No. 6,409,073 to Kaskoun, et al.

Claim 1 stands rejected under § 103(a) as being unpatentable over Smith '240 in view of Smith '102.

Applicants respectfully traverse the rejections.

Claim 1 is directed to a method for forming a semiconductor package. This method comprises:

> providing a substrate having a chip mounted thereon, the substrate having an upper surface and a lower surface opposite the upper surface, the chip being electrically connected to the upper surface of the substrate;
> forming a plurality of void pads on the back surface of the chip, the voids pads being formed of a material that is non-wettable by solder;
> applying a flux on the back surface of the chip, the flux including a solvent;
> arranging a solder preform on the flux; and
> reflowing the solder preform to form voids aligned with the void pads.

In particular, claim 1 provides a method including a reflowing of the solder preform to *form voids aligned with the void pads*.

In contrast, neither Smith '240 not Smith '120 teach or otherwise disclose this limitation. The office action states that Smith '240 discloses this limitation and points to columns 28-29; column 30, line 55 – column 31, line 21 for this disclosure. It appears that the office action is focusing on the process taught in Smith '240 where "conductive masses 1550*a* are brought to a temperature above their normal melting temperature, so that the conductive material at least partially liquefies and flows into intimate engagement with the exposed surfaces of the contacts 1519 on the dielectric sheet 1512." Column 30, lines 61-65 – referring to Fig. 25. This partial liquefying process, however, does not form any voids aligned with void pads. As the quoted citation mentions above, this process is carried out to flow the conductive material "into intimate engagement with the exposed surfaces of the contacts."

Further, any space surrounding the conductive masses is not a result of heating the conductive masses up, and in any cases does not result in the formation of voids aligned with void pads. In particular, the space surrounding the conductive masses exists simply because in forming the conductive masses on the chip, space can be left in the area not taken up by the formed conductive masses. In addition, Smith '204 teaches that "preferably after the thermally conductive masses 1550*b* are frozen, a further flowable material is added to fill the rear space 1555 between the chip rear surfaces and the heat sink." Column 31, lines 28-31. Thus, any space left by the formation of the conductive masses is filled.

Smith '102 also does not teach this limitation of claim 1. Therefore, because neither Smith '204 nor Smith '102 teach all of the limitations of claim 1, individually or in combination, they do not render claim 1 unpatentable. As such, the Applicant submits that claim 1 is in proper form for allowance, and requests that the rejection under § 103(a) be removed.

Claims 2-4 depend from claim 1. Based at least on their dependency, the Applicant submits that claims 2-4 are likewise in proper form for allowance.

*New Claims*

Claims 5-8 have been added. Claim 5 is similar to claim 1, but further clarifies that the voids formed during the reflow of the solder are formed in the solder material itself and are aligned with the void pads. Claim 6 contains limitations similar to those of claims 1 and 4 in the allowed parent application. In particular the method of claim 6 includes the formation of a conductive pattern layer and a plating layer on the back surface of the chip, while again emphasizing that the voids are formed in the thermal interface material during a reflow process.

For the foregoing reasons, reconsideration and allowance of claims 1- 6 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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